REMARKS

This is in response to the Office Action dated August 23, 2005. Examiner rejected all the claims 1-35, under 35 USC 102(e) as being anticipated by Gaudet US Patent 6,285,726. Applicants respectfully traverse this rejection and respectfully request favorable reconsideration in view of the comments set forth herein.

At the outset, applicants would like to note some fundamental distinctions between the teachings of Gaudet and the instant invention. For example, while Gaudet describes a clock recovery architecture for switches, repeaters, and multi-physical layer ports, applicants' invention relates to PLL/DLL dual loop data synchronization. More specifically, Gaudet's clock recovery architecture is a dual rate clock recovery, i.e. a clock recovery designed to run at two different data rates as described at column 1 lines 7-14. The recovered clock makes no attempt to eliminate high frequency jitter.

In contradistinction, the applicants invented a dual loop serializer comprising dual loops, one to synchronize the local clock to the received data with a wide bandwidth loop, the second to adjust the local clock to match the received data with a narrow bandwidth loop, for the purpose of frequency jitter elimination. (See paragraph 41 in the specification.)

These distinctions are succinctly set forth in the claims. For example, claim 1 recites:

A PLL/LL dual loop data serializer comprising:

a phase lock loop (PLL) including,

a phase frequency detector (PFD) receiving a local clock,

a voltage controlled oscillator (VCO),

a loop filter coupled to said PFD and to said VCO, said loop filter configured to suppress

VCO phase noise, and

a phase shifter coupled to said VCO and configured in a feedback loop with said PFD;

a delayed lock loop (DLL) having a digital loop filter coupled to a phase detector and to said phase shifter of said PLL;

a FIFO register receiving a parallel data input and outputting a signal to said phase detector; and

a PISO serializer receiving an input from said FIFO and outputting serialized data.

Certain portions of the claim have been underlined to identify items that are clearly neither taught nor suggested by the Gaudet patent. For example, since synchronization with a local clock is not an objective of Gaudet, there is no PFD receiving a local clock. Thus, if Gaudet's block 52 (in FIG. 2) is to be the equivalent of applicants' PFD, then the input (rx_data) is a data stream 54 (see column 2, lines 38 and 39) and not a local clock. By way of another example, there is no FIFO register in Gaudet that receives a parallel data input. If 20 stage shift register 154 (FIG. 5) is to be the equivalent of applicants' FIFO, this register receives Manchester encoded serial data (rxMan). Not only are these clear distinctions but, in fact, the overall combination recited in claim 1, i.e structure, operation and result are distinct from the teachings of Gaudet.

Similar distinctions are apparent in all the independent claims. By way of further example, claim 10 recites:

A method for PLL/DLL data serialization comprising:

detecting a local reference at a phase/frequency detector (PFD) of a phase lock loop (PLL);

phase locking a VCO of said PLL to a local reference to suppress a phase noise of said VCO;

receiving a parallel data input and a data clock at a FIFO register;

filtering, at a delayed lock loop (DLL), a signal representative of said fill level of said FIFO;

phase shifting an output of said VCO of said PLL in response to said filtering step;

locking said PLL to a frequency corresponding to said pre-filtered signal input to said DLL;

receiving, at a PISO serializer, said parallel data and said VCO output; and

outputting a serialized data from said PISO serializer with said VCO output a transmit clock.

As previously noted, there is no detection of a local reference at a PFD in Gaudet. The VCO of Gaudet is therefore not phase locked to a local reference. Also, the device that arguably could be the equivalent of applicants' FIFO (Gaudet's block 52 in FIG. 2) receives a serial input. Lastly, there is no suggestion anywhere in Gaudet related to filtering, at a delayed lock loop (DLL), a signal representative of said fill level of said FIFO;

By way of further illustration, claim 17 recites:

A plesiochronous data retimer comprising:

a digital delay lock loop (DDLL) receiving an input data to be retimed and configured to recover a clock of said input data;

a dual loop serializer having a phase lock loop (PLL) and a delay lock loop (DLL), said serializer comprising;

a phase/frequency detector (PFD) receiving a local reference at said PLL,

a phase shifter configured in a feedback loop with said PFD within said PLL;

a loop filter within said DLL and coupled to said phase shifter;

a SIPO (serial-in and parallel-out) deserializer coupled to said input data;

a FIFO register coupled to said deserializer and said serializer DLL; and

a PISO (parallel-in and serial-out) serializer receiving said deserialized input data and transmitting a serialized data.

As previously noted, a local reference is not received at any block identifiable as a PFD in Gaudet. There is also no phase shifter configured in a feedback loop with said PFD within said PLL. In particular, if Gaudet's delay interpolator 138 (FIG. 5) is to be equated with applicants' phase shifter, delay interpolator 138 is not in a feedback loop with the PFD within the PLL.

Claim 23 is similarly patentably distinct from Gaudet, as follows:

A plesiochrononous data retiming method comprising:

recovering a clock from a received serial input data at a digital delay locked loop (DDLL);

deserializing said serial data to a parallel data using said recovered clock;

writing said parallel data to a FIFO (first-in first-out);

synthesizing a transmit clock;

reading said parallel data from said FIFO;

serializing said parallel data using said synthesized transmit clock;

detecting a FIFO fill level at a delay locked loop (DLL); and

phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step.

Gaudet neither teaches nor suggests a plesiochronous data retiming method with writing parallel data to a FIFO or detecting a FIFO fill level at a delay locked loop.

Claim 29 also distinguishes over Gaudet, as follows:

A method for PLL/DLL data retiming comprising:

recovering a clock from a received serial input data at a digital delay locked loop (DDLL);

writing said serial data to a FIFO (first-in first-out);

synthesizing a transmit clock;

reading a retimed data from said FIFO;

detecting a FIFO fill level at a delay locked loop (DLL); and

phase shifting, in a phase lock loop (PLL), an output of a VCO, wherein said phase shifting is in response to said detecting step.

For example, Gaudet does not teach detecting a FIFO fill level at a delay locked loop.

In addition to the distinctions noted for the independent claims, all the dependent claims are believed to define a patentable invention for the same reasons and also because they recite additional features of the invention. In particular, note that claim 33 recites the step of translating said FIFO fill level to an integrating value and claim 35 recites the method of claim 29 comprising a plesiochronous system. (The Office Action provided no rationale for the rejection of claims 32-35). For the sake of completeness, it is noted that claim 23 has been amended to correct a spelling error. Lastly, the specification has been amended to insert the previously unknown serial number of the related patent application.

In view of the foregoing, all the claims in this application are believed to be in condition for allowance. An early notification of allowance is earnestly solicited.

Respectfully submitted,
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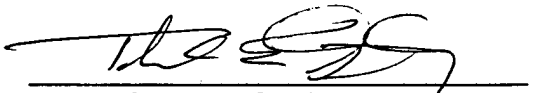

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